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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/994,982	11/26/2001	Xia Dai	P9724X	2963

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EXAMINER	
YANCHUS III, PAUL B	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 04/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/994,982	DAI, XIA	
	Examiner	Art Unit	
	Paul B. Yanchus	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 January 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5 and 10-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 10-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/31/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This non-final office action is in response to communications filed on 1/31/05.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 10-12, 15, 16, 18, 19, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al., US Patent no. 5,760,636 [Noble][1], in view of, Clark et al., US Patent no. 6,425,086 [Clark].

Regarding claim 1, Noble teaches a component comprising:

a clock generator [Clock in Figure 1] to switch from a first clock frequency [high clock frequency] to a second clock frequency [lower clock frequency] while the component is in a sleep state [processor is halted], the switch from the first to the second clock frequency to be associated with a transition between a high performance state [normal operation mode] and a low power state [low power mode, column 5, lines 27-34 and 41-49]; and

a core [Voltage Regulator in Figure 1] to receive a voltage to switch from a first voltage level [high voltage] to a second voltage level [low voltage], the switch from the first voltage level to the second voltage level to be associated with the transition between the high performance state and the low power state [column 5, lines 60-67].

Noble does not disclose that the switch from the first voltage level to the second voltage level takes place while the component is in an active mode. Clark discloses driving an internal clock of a processor directly from a PLL during a voltage level transition and processing information during the voltage level transition [column 7, lines 15-18 and 31-45]. One would be motivated to modify the Noble component to driving an internal clock of a processor directly from a PLL during a voltage level transition in order to enable the processor to continue processing information during a voltage transition [Clark, column 7, lines 31-37].

Regarding claim 2, Noble teaches that the processor is halted during a change in operating frequency. When a processor is halted, the processor does not execute instructions, but power is still supplied to the processor. Since power is still being provided to the processor during a change in operating frequency, the contents in the processor cache will be maintained during the frequency transition.

Regarding claim 3, Noble teaches adjusting the operating frequency to reduce the power consumed by a processor or other integrated circuit in a computer system [column 2, lines 49-52].

Regarding claim 4, Clark discloses that the component processes information and responds to interrupts while in the active mode [column 7, lines 31-37].

Regarding claim 5, the C0 state, as defined in the Applicant's specification, is defined as a state in which a processor executes its functions in a normal power level. Clark discloses that the component processes information and responds to interrupts while in the active mode [column 7, lines 31-37].

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[1] Included in IDS filed on 4/28/03

Regarding claim 10, Noble teaches a system comprising:

a component [Clock in Figure 1] to switch its clock frequency from a first clock frequency [high clock frequency] to a second clock frequency [lower clock frequency] while the component is in a sleep state [processor is halted], the switch from the first to the second clock frequency to be associated with a transition between a high performance state [normal operation mode] and a low power state [low power mode, column 5, lines 27-34 and 41-49]; and

a voltage regulator [Voltage Regulator in Figure 1] to switch a core voltage to the component from a first voltage level [high voltage] to a second voltage level [low voltage], the switch from the first to the second voltage level to be associated with the transition between the high performance state and the low power state [column 5, lines 60-67].

Noble does not disclose that the switch from the first voltage level to the second voltage level takes place while the component is in an active mode. Clark discloses driving an internal clock of a processor directly from a PLL during a voltage level transition and processing information during the voltage level transition [column 7, lines 15-18 and 31-45]. One would be motivated to modify the Noble component to driving an internal clock of a processor directly from a PLL during a voltage level transition in order to enable the processor to continue processing information during a voltage transition [Clark, column 7, lines 31-37].

Regarding claim 11, Noble teaches that the processor is halted during a change in operating frequency. When a processor is halted, the processor does not execute instructions, but power is still supplied to the processor. Since power is still being provided to the processor during a change in operating frequency, the contents in the processor cache will be maintained during the frequency transition.

Regarding claim 12, Noble teaches adjusting the operating frequency to reduce the power consumed by a processor or other integrated circuit in a computer system [column 2, lines 49-52].

Regarding claim 15, Noble teaches a method comprising:

switching a clock generator [Clock in Figure 1] of a component from a first clock frequency [high clock frequency] to a second clock frequency [lower clock frequency] while the component is in a sleep state [processor is halted], the switch from the first to the second clock frequency associated with a transition between a high performance state [normal operation mode] and a low power state [low power mode, column 5, lines 27-34 and 41-49]; and

switching a core voltage [Voltage in Figure 1] from a first voltage level [high voltage] to a second voltage level [low voltage], the switch from the first voltage level to the second voltage level associated with the transition between the high performance state and the low power state [column 5, lines 60-67].

Noble does not disclose that the switch from the first voltage level to the second voltage level takes place while the component is in an active mode. Clark discloses driving an internal clock of a processor directly from a PLL during a voltage level transition and processing information during the voltage level transition [column 7, lines 15-18 and 31-45]. One would be motivated to modify the Noble component to driving an internal clock of a processor directly from a PLL during a voltage level transition in order to enable the processor to continue processing information during a voltage transition [Clark, column 7, lines 31-37].

Regarding claim 16, Noble teaches that the processor is halted during a change in operating frequency. When a processor is halted, the processor does not execute instructions, but

power is still supplied to the processor. Since power is still being provided to the processor during a change in operating frequency, the contents in the processor cache will be maintained during the frequency transition.

Regarding claim 18, Noble teaches a machine-readable medium including machine-readable instructions that, if executed by a computer system, cause the computer system to perform a method comprising:

switching a clock generator [Clock in Figure 1] of a component from a first clock frequency [high clock frequency] to a second clock frequency [lower clock frequency] while the component is in a sleep state [processor is halted], the switch from the first to the second clock frequency associated with a transition between a high performance state [normal operation mode] and a low power state [low power mode, column 5, lines 27-34 and 41-49]; and

switching a core voltage [Voltage in Figure 1] from a first voltage level [high voltage] to a second voltage level [low voltage], the switch from the first voltage level to the second voltage level associated with the transition between the high performance state and the low power state [column 5, lines 60-67].

Noble does not disclose that the switch from the first voltage level to the second voltage level takes place while the component is in an active mode. Clark discloses driving an internal clock of a processor directly from a PLL during a voltage level transition and processing information during the voltage level transition [column 7, lines 15-18 and 31-45]. One would be motivated to modify the Noble component to driving an internal clock of a processor directly from a PLL during a voltage level transition in order to enable the processor to continue processing information during a voltage transition [Clark, column 7, lines 31-37].

Regarding claim 19, Noble teaches that the processor is halted during a change in operating frequency. When a processor is halted, the processor does not execute instructions, but power is still supplied to the processor. Since power is still being provided to the processor during a change in operating frequency, the contents in the processor cache will be maintained during the frequency transition.

Regarding claim 21, Noble teaches a system comprising:

in a portable unit, a component to switch a system clock frequency from a first clock frequency [high clock frequency] to a second clock frequency [lower clock frequency] while the component is in a sleep state [processor is halted], the switch from the first to the second clock frequency to be associated with a transition between a high performance state [normal operation mode] and a low power state [low power mode, column 5, lines 27-34 and 41-49]; and

a voltage regulator [Voltage Regulator in Figure 1] in the portable unit to switch a core voltage to the component from a first voltage level [high voltage] to a second voltage level [low voltage], the switch from the first voltage level to the second voltage level to be associated with the transition between the high performance state and the low power state [column 5, lines 60-67].

Noble does not disclose that the switch from the first voltage level to the second voltage level takes place while the component is in an active mode. Clark discloses driving an internal clock of a processor directly from a PLL during a voltage level transition and processing information during the voltage level transition [column 7, lines 15-18 and 31-45]. One would be motivated to modify the Noble component to driving an internal clock of a processor directly

from a PLL during a voltage level transition in order to enable the processor to continue processing information during a voltage transition [Clark, column 7, lines 31-37].

Regarding claim 22, Noble teaches that the processor is halted during a change in operating frequency. When a processor is halted, the processor does not execute instructions, but power is still supplied to the processor. Since power is still being provided to the processor during a change in operating frequency, the contents in the processor cache will be maintained during the frequency transition.

Claims 13-14, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Noble et al., US Patent no. 5,760,636 [Noble][2] and Clark et al., US Patent no. 6,425,086 [Clark], in view of, Gebara et al., US Patent no. 6,035,407 [Gebara].

Regarding claims 13, 17 and 20, Noble and Clark, as described above, teach a voltage regulator for adjusting the voltage supplied to a computer system component. Noble and Clark do not explicitly disclose how the voltage regulator adjusts the voltage supplied to the computer system component. Gebara teaches a table representation associated with a stepwise ramp that specifies that the voltage level will be adjusted by a predetermined amount of voltage at intervals of a predetermined amount of time [column 8, lines 56-60]. One would be motivated to use the Gebara voltage regulator in the Noble and Clark system to gradually adjust the voltage supplied to the computer system component in order to prevent the voltage regulator overvoltage or undervoltage circuitry from being falsely activated [Gebara, column 8, lines 60-63].

[2] Included in IDS filed on 4/28/03

Regarding claim 14, Gebara does not specifically disclose ramping the voltage in 25-50mV steps. However, Gebara does disclose gradually ramping the voltage in steps of a predetermined size and gives an example size of 100mV. It would have been obvious to one of ordinary skill in the art to reduce the voltage step size from 100mV to 25-50mV. One would be motivated enable a more gradual change from the first voltage level to the second voltage level to prevent overvoltage or undervoltage tracking circuitry form being falsely activated [column 8, lines 60-63].

Response to Arguments

Applicant's arguments with respect to claims 1-5 and 10-20 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul B. Yanchus whose telephone number is (571) 272-3678. The examiner can normally be reached on Mon-Thurs 8:00-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne H. Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul Yanchus
April 11, 2005

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SUPERVISORY PATENT EXAMINER
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